IN THE CLAIMS

1. (Currently amended) A data processing system comprising

a processor and a memory hierarchy, wherein the highest ranked level in the hierarchy is a cache coupled to the processor, wherein

a higher ranked cache in the memory hierarchy has a cache controller operating according to a write allocate scheme,

a lower ranked cache is coupled to the higher ranked cache and has a cache controller,

wherein the size of the higher ranked cache is smaller than the size of the lower ranked cache,

wherein both caches administrate auxiliary information indicating whether data present therein is valid,

~~characterized in that~~wherein,

the line size of the lower ranked cache is an integer multiple of the line size of the higher ranked cache, wherein the auxiliary information in the higher ranked cache concerns data elements at a finer granularity than ~~that~~ the auxiliary information in the lower ranked cache and wherein the higher ranked cache is arranged for transmitting a write mask to the lower ranked cache in conjunction with a line of data for indicating which data in the lower ranked cache is to be overwritten at the finer granularity, the cache controller of the lower ranked cache being arranged for fetching a cache line from the next lower ranked level in the memory hierarchy if ~~that~~ the cache line is not cached yet and the write mask indicates that the data in the line provided by the higher ranked cache is only partially valid, and wherein fetching ~~a~~the cache line from said next lower ranked level is

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suppressed if the write mask indicates that the line provided by the higher ranked cache is valid in accordance with the courser granularity of the auxiliary information in the lower ranked cache, in which case, the controller of the lower ranked cache allocates the cache line in the lower ranked cache without fetching ~~it~~the cache line from the next lower ranked level.

2. (Previously presented) Data processing system according to claim 1, comprising one or more further processors, and wherein the memory hierarchy comprises a memory having a rank which is lower than the rank of said lower ranked cache and which is shared with said other processors.

3. (Previously presented) Data processing system according to claim 1, wherein the cache lines of the lower ranked cache and the higher ranked cache have the same number of data elements.

4. (Previously presented) Data processing system according to claim 1, wherein the higher ranked cache is a write only cache.

5. (Previously presented) Data processing system according to claim 1, wherein the higher ranked cache has exactly one cache line.

6. (Currently amended) Method for operating a data processing system comprising a

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processor and a memory hierarchy, wherein the highest ranked level in the hierarchy is a cache coupled to the processor, wherein

_____a higher ranked cache in the memory hierarchy has a cache controller operating according to a write allocate scheme,

_____a lower ranked cache is coupled to the higher ranked cache and has a cache controller,

_____wherein the size of the higher ranked cache is smaller than the size of the lower ranked cache,

_____wherein both caches administrate auxiliary information indicating whether data present therein is valid,

~~characterized in that~~wherein,

the line size of the lower ranked cache is an integer multiple of the line size of the higher ranked cache, wherein the auxiliary information in the higher ranked cache concerns data elements at a finer granularity than ~~that~~ the auxiliary information in the lower ranked cache,

according to which method

the higher ranked cache transmits a write mask to the lower ranked cache in conjunction with a line of data for indicating which data in the lower ranked cache is to be overwritten at the finer granularity,

the cache controller of the lower ranked cache fetches a cache line from the next lower ranked level in the memory hierarchy if ~~that~~ the cache line is not cached yet and the write mask indicates that the data in the line provided by the higher ranked cache is only partially valid, and

wherein fetching ~~a~~the cache line from said next lower ranked level is suppressed if the write mask indicates that the line provided by the higher ranked cache is valid in accordance with the courser granularity of the auxiliary information in the lower ranked cache, in which case, the cache controller of the lower ranked cached allocates the cache line in the lower ranked cache without fetching ~~it~~the cache line from the next lower ranked level.